METHOD OF FORMING A GATE OF A NON-VOLATILE MEMORY DEVICE

ABSTRACT OF THE DISCLOSURE

A tunnel dielectric layer is formed on a semiconductor device. A floating gate layer is formed on the tunnel dielectric layer. An intergate dielectric layer (ONO layer) is formed on the floating gate layer. An in-situ doped silicon is deposited on the intergate dielectric layer to form a control gate layer and then, an annealing is carried out. The control gate layer, the intergate dielectric layer, and the floating gate layer are patterned through a photolithographic process. The phase transformation of the control gate silicon layer does not occur during a subsequent gate oxidation process to reduce the thickness variation of the ONO layer, thereby improving endurance and bake retention characteristics of the semiconductor device.